Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.016”**

**.075”**

**.075”**

**.043”**

**S**

**G**

**Top Material: Al**

**Backside Material: Ti/Ni/Au**

**G = .016” x .016”**

**S = .043 x .043”**

**Backside Potential: DRAIN**

**Mask Ref: IX11**

**APPROVED BY: DK DIE SIZE .075” X .075” DATE: 6/15/18**

**MFG: IXYS THICKNESS .012” P/N: IXTD1R6N50**

**DG 10.1.2**

#### Rev B, 7/1